Satellite front ends

SF910 family

APPLICATION

The SF910 satellite front end family is designed to cover all frequencies in the range of 950 MHz to 1750 MHz. They are meant for both D-/D2-MAC DBS and PAL/SECAM FSS signals.
The SF910 has a built-in digitally controlled (I^2C-bus) PLL tuning system. The IF-part is equipped with a PLL demodulator IC.

The D-version has a dual switchable input which is controlled via an I^2C-bus. The SF914 and SF914D meet the requirements for radiation in accordance with the amendment to CENELEC EN55013 (57 dBpW).

DESCRIPTION

These satellite front ends are a combination of a tuner covering a frequency range of 950 MHz to 1750 MHz and an IF signal processing unit.
The tuner is fitted with a broadband matching network followed by an RF amplifier which is loaded with an electronically tuned bandpass filter. The selected channel is mixed with a synthesized oscillator signal to obtain an intermediate frequency (IF) which in turn passes to a filter and a gain controlled amplifier.
The IF unit contains a SAW filter followed by a buffer amplifier and a PLL FM-demodulator. The demodulated signals are applied to a video buffer amplifier to drive the video signal processing circuit.

The unit is mounted in a metal housing with front and rear covers.

QUICK REFERENCE DATA

System	D-/D2-MAC, PAL, SECAM
Frequency band	950 MHz to 1750 MHz
Channels	1 to 40 in accordance with WARC77
Intermediate frequency (note 1)	479.5 MHz
Baseband video polarity	positive

Note

1. The oscillator frequency is higher than the aerial signal frequency.

AVAILABLE VERSIONS

TYPE	INPUT CONNECTOR(S)	AMTSBLATT/ CENELEC	CATALOGUE NUMBER
SF912	IEC (female)	no	
SF912D	IEC (female) and IEC (male)	no	
SF914	IEC (female)	yes	3122 237 10551
SF914D	IEC (female) and IEC (male)	yes	3122 237 10561

BLOCK DIAGRAM

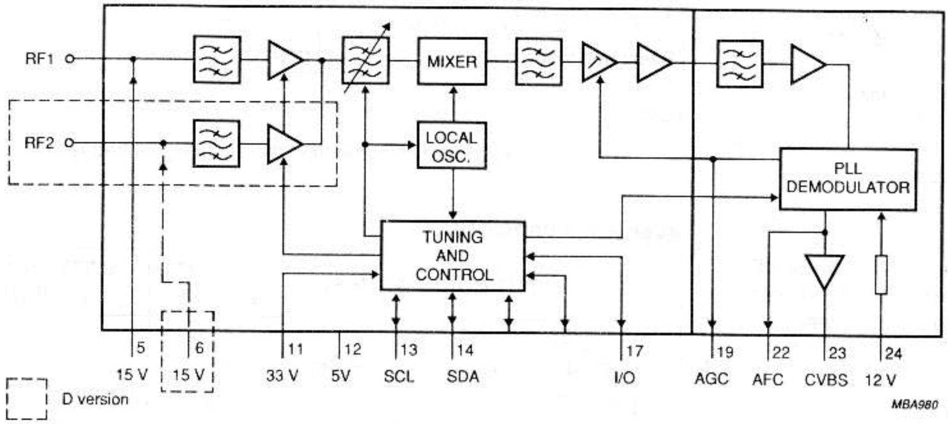


Fig.1 Block diagram.

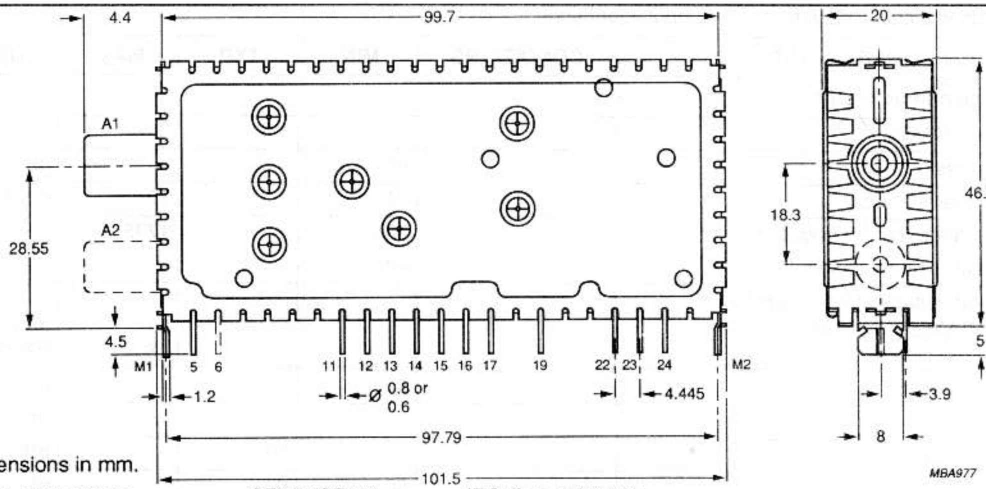
PINNING

PIN	FUNCTION
A1	aerial input 1 (female)
A2	aerial input 2 (male, D-version)
5	LNC voltage supply
6	LNC voltage supply (D-version)
11	tuning voltage supply
12	tuner section voltage supply
13	SCL (serial clock line) I^2C-bus control
14	SDA (serial data line) I^2C-bus control
17	I/O (input/output) port
19	AGC output
22	AFC output
23	CVBS baseband output
24	IF section voltage supply
M1	mounting tag
M2	mounting tag

SEMICONDUCTOR COMPONENT LIST

RF transistor	BFG93AR
PIN diode	HVR187
Mixer transistor	BFR92A
Oscillator transistor	BFR93A
Tuning diodes	BB811
PLL tuning IC	SP5055S
IF transistors	BFR92A + BFS01R
IF amp IC	µPC1688G
SAW filter	B529
PLL demodulator IC	TDA8730
Varicap diode	OF4199
Video transistor	BC848B

MECHANICAL DATA



Dimensions in mm.

Aerial connection:

SF912/SF914	IEC (female) 75 Ω
SF912D/SF914D	IEC (female) / IEC (male) 75 Ω

Fig.2 Mechanical outline.

ELECTRICAL DATA

Unless otherwise specified all electrical values apply at an ambient temperature of 25 ±5 °C, a relative humidity of 60 ±10%, tuner and PLL supply voltages at 5 ±0.2 V, an IF supply voltage of 12 ±0.3 V and a tuning supply voltage of 33 ±0.5 V via a 22 Ω series resistor. See note 1.

PARAMETER	TYP.	MAX.	UNIT
Voltages and currents			
Tuner section voltage supply	5 ±5%	–	V
Current drawn from +5 V supply	–	150	mA
IF section voltage supply	12 ±5%	–	V
Current drawn from +12 V	–	132	mA
Tuning voltage supply (note 2)	33	–	V
Tuning voltage supply current	–	1.7	mA
LNC voltage supply	–	20	V
LNC voltage supply current	–	400	mA

Notes

1. The front end is tuned by means of a built-in I^2C-bus controlled synthesizer. For further information refer to Application Information.
2. An external pull-up resistor of 22 kΩ ±5% must be connected between the tuning voltage supply and pin 11.

CHARACTERISTICS

All specified input levels refer to 75 Ω input impedance.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF input characteristics					
In-band VSWR		–	1.5	3	
Return loss		6	–	–	dB
RF input level range		44	–	79	dBμV
Tuning range (carrier frequency) Margin at extreme channels		965 20	– –	1735 –	MHz MHz
Oscillator voltage at aerial input from 40 MHz to 1750 MHz from 1750 MHz to 2250 MHz		 – –	 – –	 54 76	 dBμV dBμV
Surge protection		5	–	–	kV
Noise figure		–	10	15	dB
Image rejection		35	50	–	dB
IF rejection		50	60	–	dB
Channel 1 in-channel intermodulation		79	85	–	dBμV
In-band intermodulation		79	–	–	dBμV
AFC output characteristics					
DC level when correctly tuned		3	3.4	3.8	V
Slope detuning		–	90	–	mV/MHz
Time constant		–	22	–	ns
AGC output characteristics					
Output impedance		–	10	–	kΩ
Output load		100	–	–	kΩ
Output level range for 79 dBμV unmodulated RF input signal for 44 dBμV unmodulated RF input signal		 – –	 3.5 7.5		 V V
Baseband output					
Baseband output load		–	470	–	Ω
DC level		1.8	2.3	2.8	V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL video characteristics (measurement conditions, unless otherwise specified)					
RF input level		–	60	–	dBμV
Carrier-to-noise ratio	measured in 27 MHz bandwidth	30	–	–	dB
MODULATION PARAMETERS					
Frequency deviation	CCIR-405 pre-/de-emphasis PAL coded video signal positive modulation	–	25	–	MHz/V
Video output level	no de-emphasis, measured from top sync to peak white	–	550	–	mV
Baseband frequency response	maximum amplitude deviation between 0.1 MHz and 5 MHz	–	–	0.5	dB
Dynamic threshold	the C/N limit at which clicks in a 75% saturated colour bar are just visible	–	–	13	dB
Static threshold		–	5	–	dB
Unweighted signal-to-noise ratio	C/N = 14 dB	39	40	–	dB
Differential phase	frequency deviation 16 MHz/V	–	±2	±5	deg
Differential gain	frequency deviation 16 MHz/V	–	±2	6	%
Second order intermodulation (The level difference between a 3.25 MHz video carrier and its second harmonic at 6.5 MHz)		25	30	–	dB
MAC video characteristics					
MODULATION PARAMETERS					
Frequency deviation	EBU pre-/de-emphasis D2-MAC coded video signal	–	13.5	–	MHz/V
Video output level	measured from black to white luminance level (no de-emphasis)	–	700	–	mV
Baseband frequency response	maximum amplitude deviation between 0.1 MHz and 10 MHz	–	–	1	dB
Dynamic threshold	the C/N limit at which clicks in a 75% saturated colour bar are just visible	–	–	9	dB
Bit error rate	C/N value for BER = 10^{-3}	–	–	8	dB
	C/N value for BER = 10^{-5}	–	–	11	dB

LOGIC TABLES

READ MODE ($R/\overline{W}$ = 1)

Table 1

	MSB							LSB
Address byte	1	1	0	0	0	MA1	MA0	$R/\overline{W}$
Status byte	POR	FL	I2	I1	I0	A2	A1	A0

Status byte explanation

POR	Power on reset indicator, set to logic 1 if the power supply to the device has dropped below 3 V
	The POR is set to 0 when the read sequence is terminated by a stop command
FL	Phase Lock Detect Flag:
	1 = device is phase locked
	0 = device is unlocked
I2	No relevant information
I1, I0	Status ports P5 and P4
	0 indicates LOW level
	1 indicates HIGH level
A2, A1, and A0	5 level A/D converter data from P6, can be used to feed AFC information from the IF section to the microprocessor

Telegram examples

READ MODE FROM PROCESSOR

Table 2

Start	Adr	Ack	STB	Ack	STB		Stop
Start	Adr	Ack	STB		Stop		

From PLL

No acknowledge	end of data
Start	start condition
Adr	address
Ack	acknowledge
STB	status byte
Stop	stop condition

WRITE MODE (R/$\overline{W}$ = 0)

Table 3

	MSB							LSB
Address byte	1	1	0	0	0	MA1	MA0	R/$\overline{W}$
Prog. div. byte1	0	n14	n13	n12	n11	n10	n9	n8
Prog. div. byte 2	n7	n6	n5	n4	n3	n2	n1	n0
Control byte 1	1	CP	T1	T0	1	1	1	OS
Control byte 2	P7	P6	P5	P4	P3	P2 (note 1)	P1 (note 1)	P0

Note

1. P1 and P2 not connected in the IC package.

Address

The address of the front end is fixed to C6: (MA1, MA0) = (1, 1) and also responds to C2: (MA1, MA0) = (0, 1)

Programmable divider setting	
Divider ratio	$N = 16 \times (f_{rf,pc} + f_{if,pc})$ (MHz) $F_{osc} = N / 16$ (MHz) N = (16384 x n14) + (8192 x n13) + (4096 x n12) + (2048 x n11) + (1024 x n10) + (512 x n9) + (256 x n8) + (128 x n7) + (64 x n6) + (32 x n5) + (16 x n4) + (8 x n3) + (4 x n2) + (2 x n1) + (n0)
Control byte 1	
Charge pump setting	CP can be set to either 0 (LOW current) or 1 (HIGH current). CP = 1 results in fastest tuning
Test mode setting	T1, T0 = 0 for normal operation
PLL disabling	OS = 0 for normal operation OS = 1 switches the charge pump transistor to a non-conducting state, the front end can then be tuned manually with a variable tuning voltage applied to pin 11 When selecting OS = 1, it is recommended to set simultaneously T0 = 1.
Control byte 2	
Port P0 to P5	not used
Port P6	I/O port 3 0 for HIGH impedance output 1 for LOW impedance output If the port is to be used as an input port it should not be programmed to output a LOW impedance state
Port P7	for single input version: P7 = 0 for normal operation for dual input version (antenna input select) P7 = 0 for input RF1 P7 = 1 for input RF2

Telegram examples

WRITE MODE

Table 4

Start	Adr	Ack	DIV1	Ack	DIV2	Ack	CB1	Ack	CB2	Ack	Stop
Start	Adr	Ack	DIV1	Ack	DIV2	Ack	CB1	Ack	CB2	Ack	Stop
Start	Adr	Ack	DIV1	Ack	DIV2	Ack	DIV1	Ack	Stop		
Start	Adr	Ack	DIV1	Ack	DIV2	Ack	Stop				
Start	Adr	Ack	CB1	Ack	CB2	Ack	Stop				
Start	Adr	Ack	CB1	Ack	CB2	Ack	DIV1	Ack	Stop		

key

Start	start condition
Adr	address
Ack	acknowledge
DIV1	divider ratio byte 1
DIV2	divider ratio byte 2
CB1	control byte 1
CB2	control byte 2
Stop	stop condition

APPLICATION INFORMATION

I²C-bus control

For further information regarding general aspects of I²C-bus control, refer to *"The I²C-bus specification"* published by Philips Components.

AFC system

An example of a simple AFC system for the front end in combination with an interface circuit is briefly described below.

The system makes use of the internal A/D converter of the PLL frequency synthesizer in the tuner part.

The AFC signal coming out on pin 22 is applied to a simple first order lowpass filter (R4 - C) to remove the video and frequency dispersal signal in order to obtain a DC signal that is a measure for the centre frequency of the FM signal entering the demodulator. With R4 = 470 kΩ and C = 100 nF a suitable lowpass filter is obtained.

A simple low frequency operational amplifier is used to make a DC level shift and slope adjustment so that the output (V_O) matches the A/D converter window. The A/D converter has 5 levels ranging from 000 to 100 with the mid level 010 corresponding to the window centre around 1.88 V and a window of about 750 mV. For a tuning accuracy of ±1 MHz, a 2 MHz frequency window is required. With the demodulator slope of about 85 mV/MHz, a 2 MHz window at the AFC output equals 170 mV. Therefore the interface circuit must provide a gain of 750 mV/170 mV = 4.41.

The resistors can be calculated from the following equations:

$$G = (1 + R1) \div Rx$$

$$Rx = R2 + R3^{+} \times R3^{-} \div (R3^{+} + R3^{-})$$

where:

$R3^{+}$ is the value between the wiper of R3 and V_S

$R3^{-}$ is the value between the wiper of R3 and ground

$$V_O = (V1 \times G) - (V_S \times R1 \times R3^{-}) \div (Rx \times R3)$$

The digital values from the A/D converter output can be read via the I²C-bus and processed by the microcontroller that controls the tuning system. The software for the AFC tuning system must be able to handle a curve shown in Fig.4.

A demonstration software package is available from Philips Components for controlling all tuning functions of a PLL synthesized tuning system for satellite receivers. It requires a MS-DOS operating system and runs on IBM PC/XT/AT computers or compatibles. For control of the I²C-bus an interface board is required which is plugged into the computer's Centronics port.

Mounting the unit on a printed wiring board (PWB)

The unit must be mounted on the board ensuring that there is no clearance between the supporting surfaces and the PWB.
In this condition the unit is soldered in place.

This can be achieved by:

(a) Pressing the unit vertically on the PWB during soldering

(b) Supporting the unit with its aerial connector in the right position

(c) Twisting the ground tags (see Fig.5).

In order to prevent any stress to the PWB it is recommended that the unit is supported at its aerial connector.

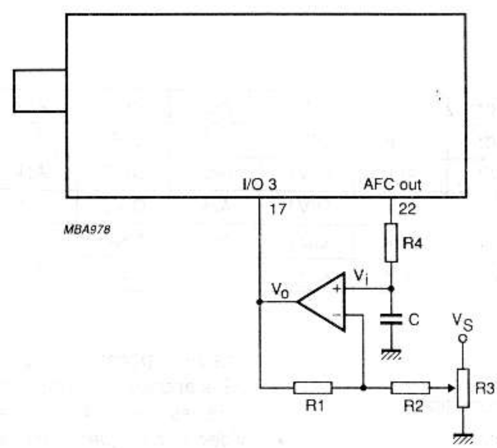


Fig.3 AFC interface circuit.

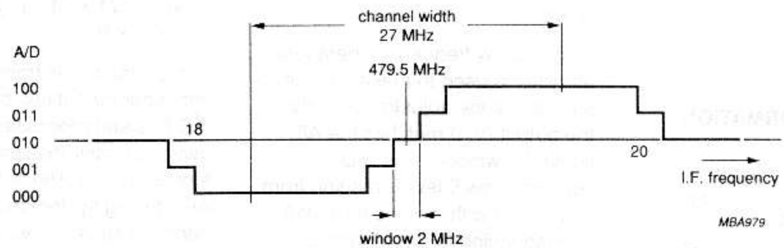
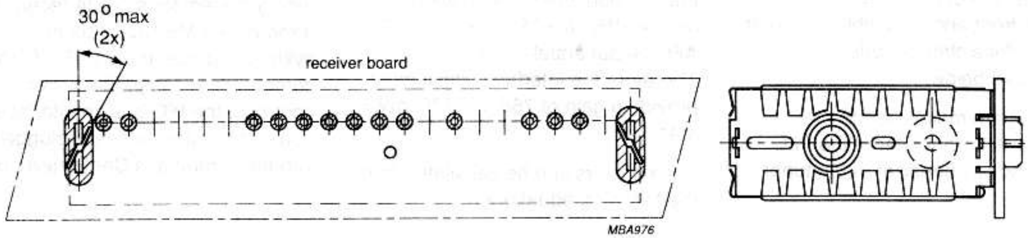
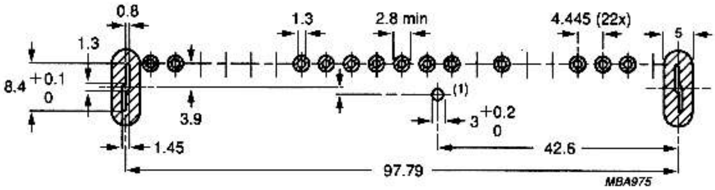


Fig.4 A/D converter window.



Viewed from the solder side.

Fig.5 Lug twist method of mounting tabs.



Dimensions in mm.

Viewed from the solder side.

(1) Additional hole for extra fixing with a pan tap screw 2N. max length 4.05 mm.

Fig.6 Piercing diagram.